Preliminary Datasheet

N-Channel 60-V (D-S) MOSFET

FEATURES

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

PRODUCTY SUMMARY			
V_{DS}	$R_{DS(on)}$ m(Ω)		I_D(A)
60	46	Rdson @-10V	4.8
	54	Rdson @-4.5V	4.5

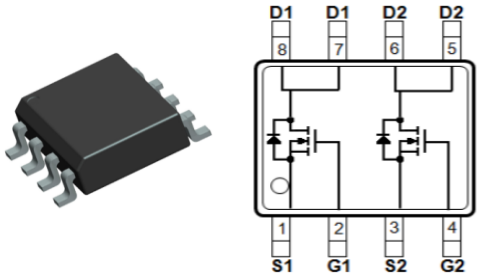
Application

- Portable Devices
- Consumer Electronics

Mechanical

- Case: SOP-8-Dual Package

SOP-8-Dual



Packing Information

Package	Packing
SOP-8-Dual	3K/13" Reel

Maximum Ratings (T_A=25°C unless otherwise specified)			
Parameter	**Symbol**	**Limit**	**Unit**
DrainSource Voltage	V_{DS}	60	V
GateSource Voltage	V_{GS}	±20	V
Continuous Drain Current [4)]	I_D	5	A
Maximum Power Dissipation	P_D	1.2	W
Pulsed Drain Current [1)]	I_{DM}	20	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	55~150	°C

Typical Thermal Resistance			
Parameter	**Symbol**	**Limit**	**Unit**
JunctiontoAmbient Thermal Resistance	$R_{\theta JA}$	62.5	°C/W

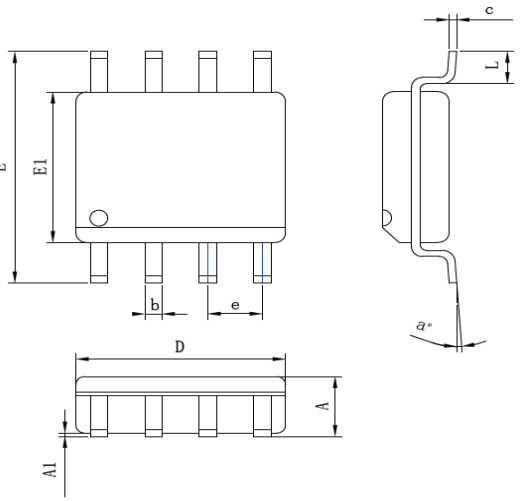
NOTES :
1. Pulse width<300us, Duty cycle<2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ =25°C.
4. The maximum current rating is package limited.
5. RQJA is the sum of the junctiontocase and casetoambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch2 with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

Electrical Characteristics (T_A = 25°C UNLESS OTHERWISE NOTED)						
Characteristics	Symbol	Test Condition	Limits			Unit
			Min	Typ	Max	
Static						
DrainSource Breakdown Voltage	B_{VDSS}	V_{GS} = 0V, I_D =250uA	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.00	1.60	3.00	V
DrainSource OnState Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4.8A	-	40	46	mΩ
		V_{GS}=4.5V, I_D=4.5A	-	46	54	mΩ
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	uA
GateSource Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Dynamic [3]						
Total Gate Charge	Q_g	VDS = 30 V, VGS = 4.5 V, ID = 5.4 A	-	16	-	nC
GateSource Charge	Q_{gs}		-	3.9	-	nC
GateDrain Charge	Q_{gd}		-	8.2	-	nC
Input Capacitance	C_{iss}	VDS = 15 V, VGS = 0 V, f = 1 MHz	-	1460	-	pF
Output Capacitance	C_{oss}		-	125	-	pF
Reverse Transfer Capacitance	C_{rss}		-	110	-	pF
Switching						
TurnOn Delay Time	$t_{d(on)}$	VDS = 30 V, RL = 5.6 Ω, ID = 5.4 A, VGEN = 10 V, RGEN = 6 Ω	-	8	-	ns
TurnOn Rise Time	t_r		-	9	-	ns
TurnOff Delay Time	$t_{d(off)}$		-	49	-	ns
TurnOff Fall Time	t_f		-	14	-	ns
DrainSource Diode						
Maximum Continuous Body Diode Forward Current	I_S	VG=VD=0V , Force Current	-	-	1.2	A
Diode Forward Voltage	V_{SD}	IS=1.0A, VGS=0V	-	-	1.5	V

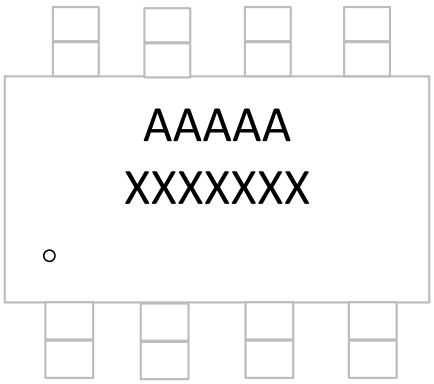
Note:
1. Pulse width<300us, Duty cycle<2%
2. Fused current that based on wire numbers and diameter
3. Guaranteed by design, not subject to production testing.

Package Outline Dimensions (inches and millimeters)

SOP-8				
SYMBOL	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.75		0.069
A1	0.10	0.23	0.004	0.009
b	0.35	0.48	0.014	0.019
c	0.19	0.25	0.007	0.010
D	4.70	5.10	0.185	0.201
E	5.80	6.20	0.228	0.244
E1	3.70	4.10	0.146	0.161
e	1.27bsc			
L	0.50	0.80	0.020	0.031
a °	0 °	8 °	0 °	8 °



Marking Information



First line:

AAAAA = Product number

XXXXXXX = Tracking number

Third line:Gate Pin Point

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