

V1.1 Datasheet

N-Channel 100V MOSFET

FEATURES

- ●Trench Process Technology
- ●Ultra Low On-resistance Design

PRODUCTY SUMMARY						
V _{DS} (V)	I _D (A)	$R_{DS(on)} m(\Omega) Max$				
100	360	1.25	@V _{GS} =10V			
100	300	2.2	@V _{GS} =6V			

Application

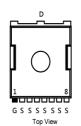
- ●BMS Application
- ●Consumer Electronics

Mechanical

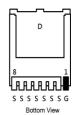
●Case:TOLL Package

G S

TOLL







Packing Information

Package	Packing	
TOLL	2K/13" Reel	

Maximum Ratings (T _A =25°C unless otherwise specified)						
Param	Symbol	Limit	Unit			
Drain-Source Voltage		V_{DS}	100	V		
Gate-Source Voltage		V_{GS}	±20	V		
Continuous Drain Current 2)	T _C =25°C	-	401	А		
	T _C =100°C	I _D	254	А		
Pulsed Drain Current 1)	T _C =25°C	I _{DM.pulesd}	1440	А		
Avalanche Energy ⁶⁾		E _{AS}	1806	mJ		
D D: : ::	T _C =25°C	D	500	W		
Power Dissipation	Derating Factor above 25°C	P_{D}	4	W/°C		
Operating Junction and Storage	Temperature Range	T _J , T _{STG}	150, -55 to 150	°C		
Maximum Temperature for Soldering		T _L	260	°C		

Typical Thermal Resistance						
Parameter	Symbol	Limit	Unit			
Junction-to-Ambient Thermal Resistance 5)	$R_{ heta JA}$	62.5	°C/W			
Junction-to-Case Thermal Resistance	$R_{ heta JC}$	0.25	°C/W			

Note:

- 1. Pulse width limited by maximum junction temperature. Pulse width<300us, Duty cycle<2%.
- 2. Fused current that based on wire numbers and diameter.
- 3. Guaranteed by design, not subject to production testing.
- 4. The maximum current rating is package limited.
- 5. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ =150°C. Ratings are based on low frequency and duty cycles to keepinitial T_J =25°C.
- 6. L=0.5mH, I_{AS} =85A, Start T_J =25°C



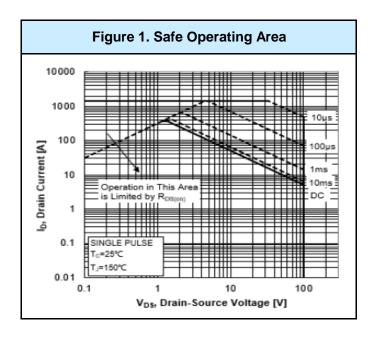
	Symbol Test Condition	Limits			Unit		
Characteristics	Symbol	rest Condition	Min	Тур	Max	Offic	
		Static Characteristics					
Drain-Source Breakdown Voltage	B_{VDSS}	V _{GS} =0V, I _D =250uA	100	-	-	V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=250uA$	2.0	3.0	4.0	V	
D : 0	D	V _{GS} =10.0V, I _D =50A	-	1.1	1.25	mΩ	
Drain-Source On-State Resistance ¹⁾	R _{DS(on)}	V _{GS} =6.0V, I _D =20A	-	1.7	2.2	mΩ	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA	
GateSource Leakage Current	I _{GSS}	V_{GS} =±20V, V_{DS} =0V	-	-	±100	nA	
	Dy	ynamic Characteristics 3)		_			
Input Capacitance	C _{iss}		-	14200	-	pF	
Output Capacitance	C _{oss}	V_{DS} =50V, V_{GS} =0V, f=1MHz	-	4000	-		
Reverse Transfer Capacitance	C_{rss}		-	935	-		
Total Gate Charge ²⁾	Q_g		ı	240	-	nC	
Gate-Source Charge ²⁾	Q_{gs}	V _{DS} =50V, V _{GS} =10V, I _D =50A	-	64	-		
Gate-Drain Charge ²⁾	Q_{gd}		-	64	-		
	I	Switching					
Turn-On Delay Time ²⁾	t _{d(on)}		-	45	-		
Turn-On Rise Time ²⁾	t _r	$V_{DD} = 50V, V_{GS} = 10V, R_{G} = 1.6\Omega$	-	51	-	ns	
Turn-Off Delay Time ²⁾	t _{d(off)}	bb 7 dd 7 d	-	123	-		
Turn-Off Fall Time ²⁾	t _f		-	52	-		
Maximum Continuous Body Diode	ı	Drain-Source Diode					
Forward Current	I _S	-	-	-	360	Α	
Maximum Pulsed Current	I _{SM}	-	-	-	1440	А	
Diode Forward Voltage ¹⁾	V_{SD}	I _S =50A, V _{GS} =0V	-	-	1.2	V	
Reverse Recovery Time	t _{rr}	L _50A & /d _100A/us	-	87	-	nS	
Reverse Recovery Charge	Q _{rr}	$I_F = 50A$, $d_{IF}/d_t = 100A/\mu S$	-	220	-	nC	

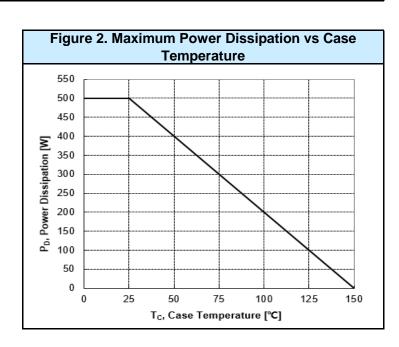
Note:

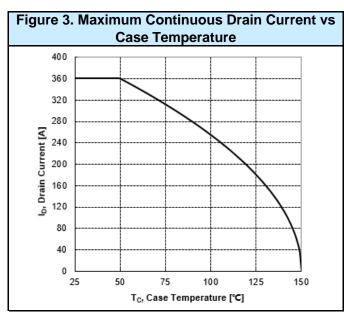
- 1. Pulse width<300us, Duty cycle<2%.
- 2. Essentially independent of operating temperature typical characteristics.
- 3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ =150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
- 4. The maximum current rating is package limited.
- 5. R_{eJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch2 with 2oz.square pad of copper.
- 6. Guaranteed by design, not subject to production testing.

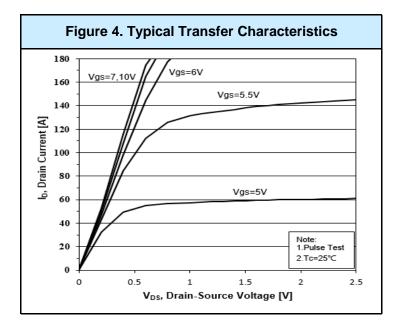


Typical Characteristic Curves

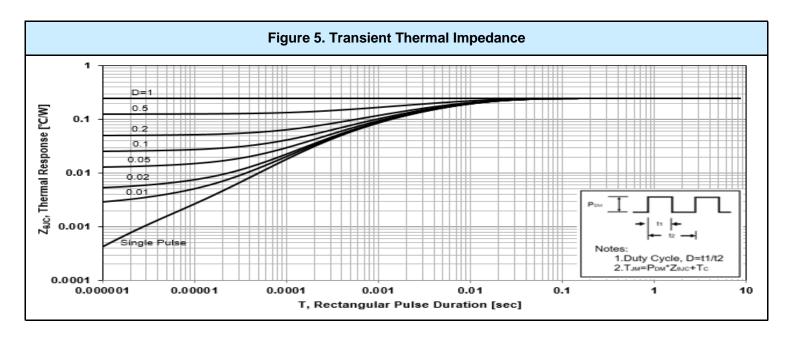


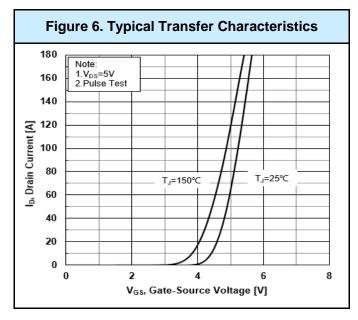


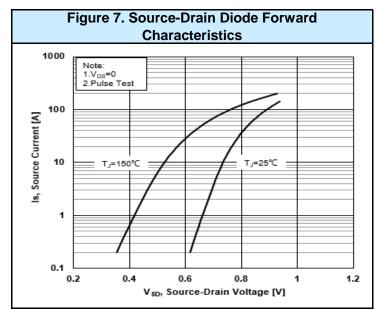




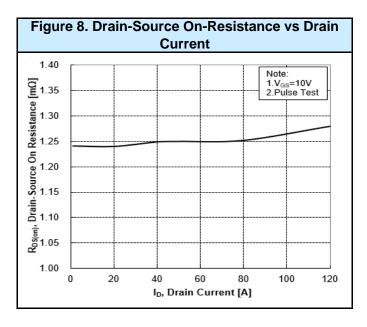


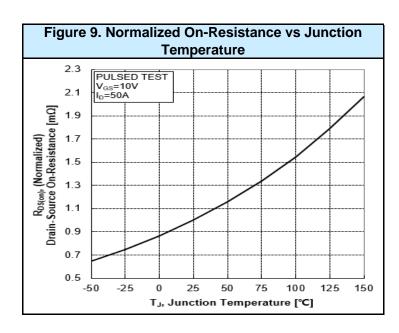


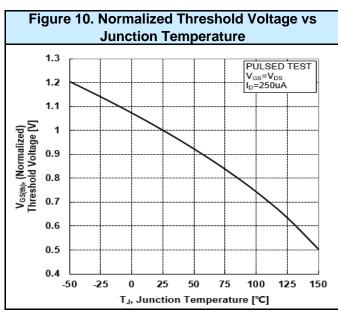


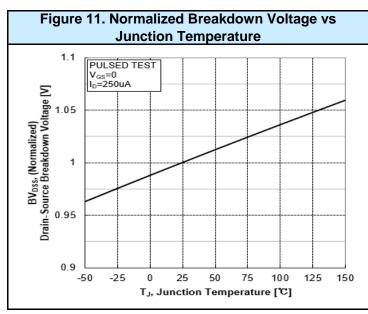


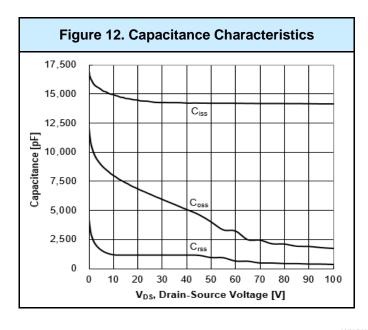


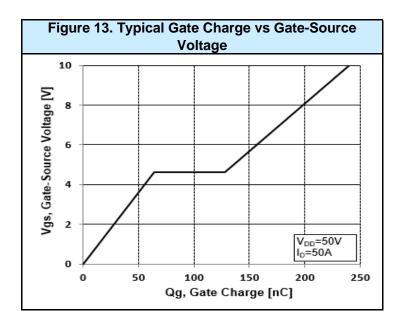








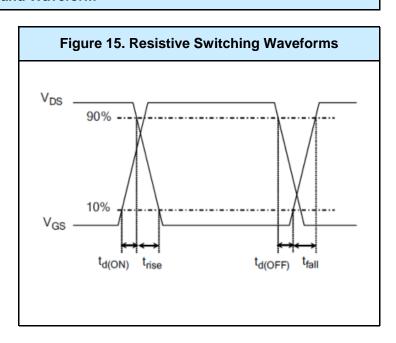


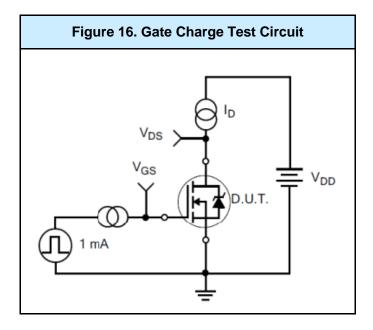


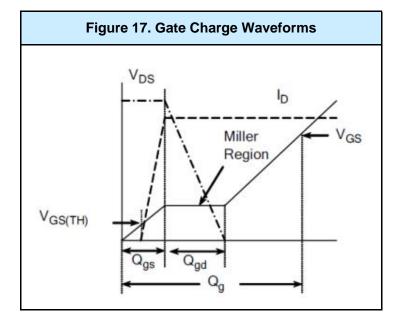


Test Circuit and Waveform

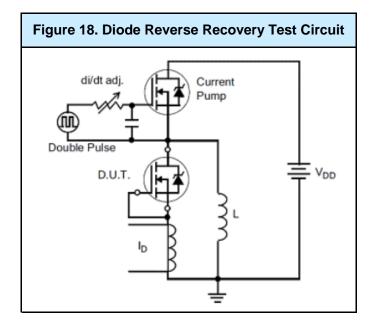
Figure 14. Resistive Switching Test Circuit

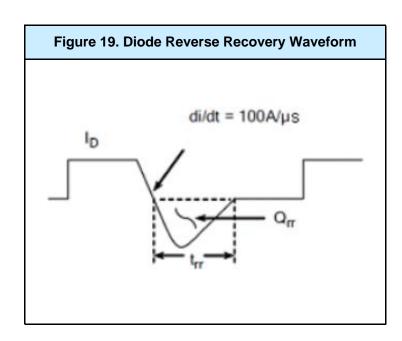


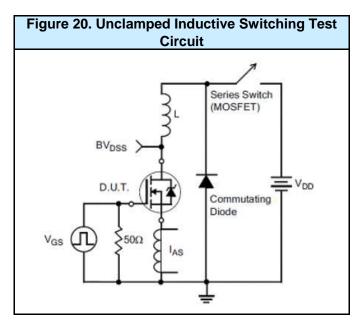


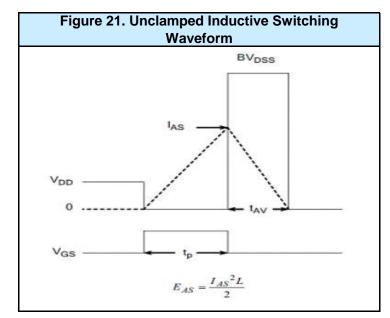








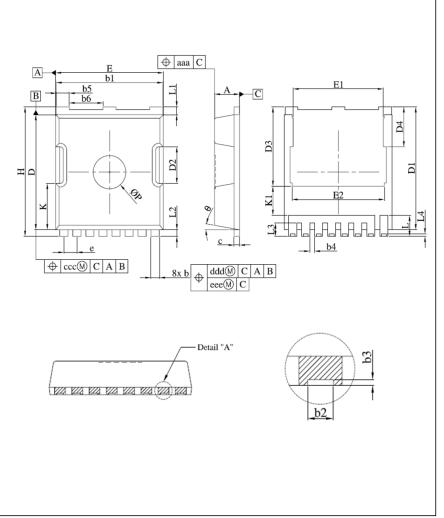




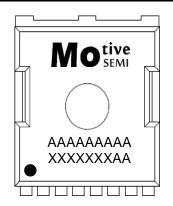


Package Outline Dimensions (inches and millimeters)

	_				
TOLL					
	Dimensions				
SYMBOL	Millimeters		Inches		
	Min	Max	Min	Max	
Α	2.20	2.40	0.087	0.094	
b	0.70	0.90	0.028	0.035	
b1	9.70	9.90	0.382	0.390	
b2	0.36	0.55	0.014	0.022	
b3	0.05	0.35	0.002	0.014	
b4	0.30	0.50	0.012	0.020	
b5	1.10	1.30	0.043	0.051	
b6	3.00	3.20	0.118	0.126	
С	0.40	0.60	0.016	0.024	
D	10.28	10.55	0.405	0.415	
D1	10.98	11.18	0.432	0.440	
D2	3.20	3.40	0.126	0.134	
D3	7.00	7.30	0.276	0.287	
D4	3.44	3.74	0.135	0.147	
е	1.10	1.30	0.043	0.051	
Е	9.80	10.00	0.386	0.394	
E1	8.20	8.40	0.323	0.331	
E2	8.35	8.65	0.329	0.341	
Н	11.50	11.85	0.453	0.467	
K	4.08	4.28	0.161	0.169	
K1	2.45	-	0.096	-	
L	1.60	2.10	0.063	0.083	
L1	0.50	0.90	0.020	0.035	
L2	0.50	0.70	0.020	0.028	
L3	1.00	1.30	0.039	0.051	
L4	0.13	0.33	0.005	0.013	
Р	2.85	3.15	0.112	0.124	
θ		10° I	REF.		
aaa	0.2	20	0.008		
ccc	0.2	20	0.008		
ddd	0.2	25	0.010		
eee	0.2	20	0.008		



Marking Information



First line = Company name

AAAAAAAA = Product number

XXXXXXX = Tracking number

Fourth line = Gate pin point

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