MSN0340N

V1.4 Datasheet

N-Channel 40V MOSFET

FEATURES

●Advance Trench Process Technology

●High Density Cell Design for Ultra Low On-resistance

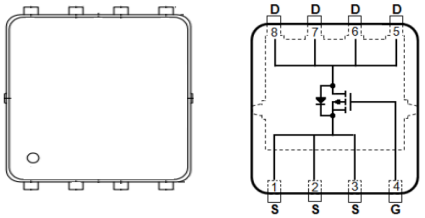
PRODUCTY SUMMARY			
V_{DS} (V)	I_D (A)	$R_{DS(on)}$ m(Ω) Max	
40	110	2.55	@V_{GS}=10V
		3.5	@V_{GS}=4.5V

Application

●DC - DC Converter

●Motor drivers

DFN5060



Mechanical

●Case:DFN5060 Package

Packing Information

Package	Packing
DFN5060	3K/13" Reel

Maximum Ratings (T_A=25°C unless otherwise specified)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1)3)]	T_C=25°C	I_D	110	A
Continuous Drain Current [1)3)]	T_C=100°C	I_D	69	A
Continuous Drain Current [1)3)]	T_C=100°C	I_{DM}	320	A
Maximum Power Dissipation [1)]		P_{tot}	35	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Typical Thermal Resistance			
Parameter	**Symbol**	**Limit**	**Unit**
Junction-to-Case Thermal Resistance [3)]	$R_{\theta JC}$	3.5	°C/W
Junction-to-Ambient Thermal Resistance [3)]	$R_{\theta JA}$	62.5	°C/W

Note:
1. Pulse Test: Pulse Width≤300 μs, Duty Cycle≤2%
2. Fused current that based on wire numbers and diameter.
3. Guaranteed by design, not subject to production testing.
4. The maximum current rating is package limited.
5. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keepinitial T_J =25°C.

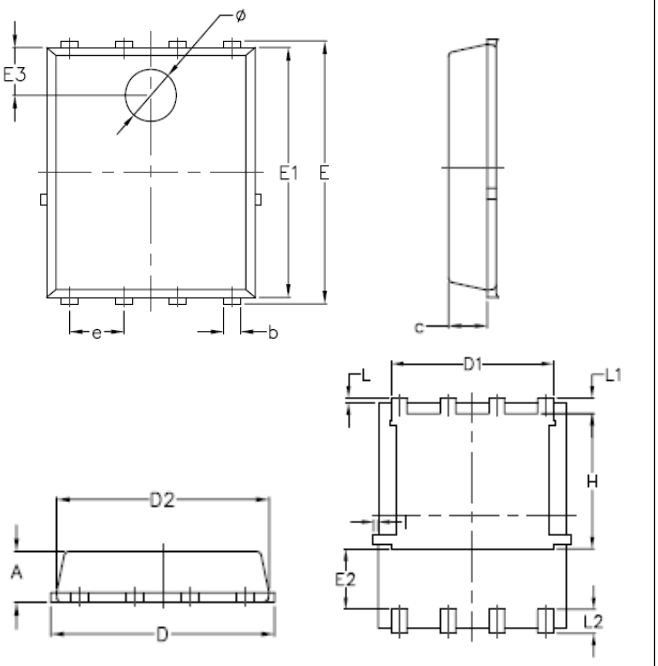
Electrical Characteristics (T_A = 25°C UNLESS OTHERWISE NOTED)						
Characteristics	Symbol	Test Condition	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250uA	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.00	1.40	2.50	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10.0V, I_D=20.0A	-	2.38	2.55	mΩ
		V_{GS}=4.5V, I_D=20.0A	-	2.8	3.5	mΩ
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1.0	uA
GateSource Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic [3]						
Total Gate Charge	Q_g	V_{DS}=20V, V_{GS}=10V, I_D=1.0A	-	185	-	nC
Total Gate Charge	Q_g	V_{DS}=20V, V_{GS}=4.5V, I_D=1.0A	-	91	-	nC
Gate-Source Charge	Q_{gs}		-	15	-	nC
Gate-Drain Charge	Q_{gd}		-	36	-	nC
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V, f=200KHz	-	9839	-	pF
Output Capacitance	C_{oss}		-	627	-	pF
Reverse Transfer Capacitance	C_{rss}		-	635	-	pF
Switching						
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=20V, R_L=10.0Ω, V_{GEN}=10V, R_G=3.0Ω	-	26	-	ns
Turn-On Rise Time	t_r		-	23	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	209	-	ns
Turn-Off Fall Time	t_f		-	59	-	ns
Drain-Source Diode						
Body-Diode Continuous Current	I_S	-	-	-	110	A
Diode Forward Voltage [1]	V_{SD}	I_{SD}=20A, V_{GS}=0V	-	-	1.5	V

Note:
1. Pulse width<300us, Duty cycle<2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
4. The maximum current rating is package limited.
5. R_{QJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch2 with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

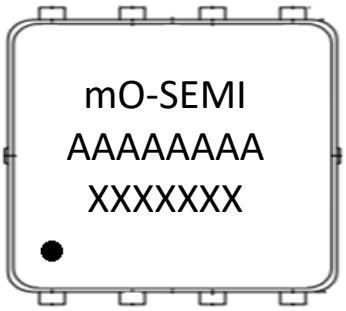
Package Outline Dimensions (inches and millimeters)

DFN5060

SYMBOL	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A	1.03	1.17	0.041	0.046
b	0.34	0.48	0.013	0.019
c	0.82	0.97	0.032	0.038
D	4.80	5.40	0.189	0.213
D1	4.11	4.31	0.162	0.170
D2	4.80	5.00	0.189	0.197
E	5.95	6.15	0.234	0.242
E1	5.65	5.85	0.222	0.230
E2	1.40	-	0.055	-
E3	1.00	1.20	0.039	0.047
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.002	0.010
L1	0.38	0.50	0.015	0.020
L2	0.38	0.71	0.015	0.028
H	3.30	3.50	0.130	0.138
I	-	0.18	-	0.007
Φ	1.10	1.30	0.043	0.051



Marking Information



First line = Company name

AAAAAAAAAA = Product number

XXXXXXX = Tracking number